Targeted Fault Tolerance By Special CPU Instructions
Inventor(s): Ken Gary Pomaranski, et al.
Serial No. 10/623,099

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FIG. 1

Targeted Fault Tolerance By Special CPU Instructions
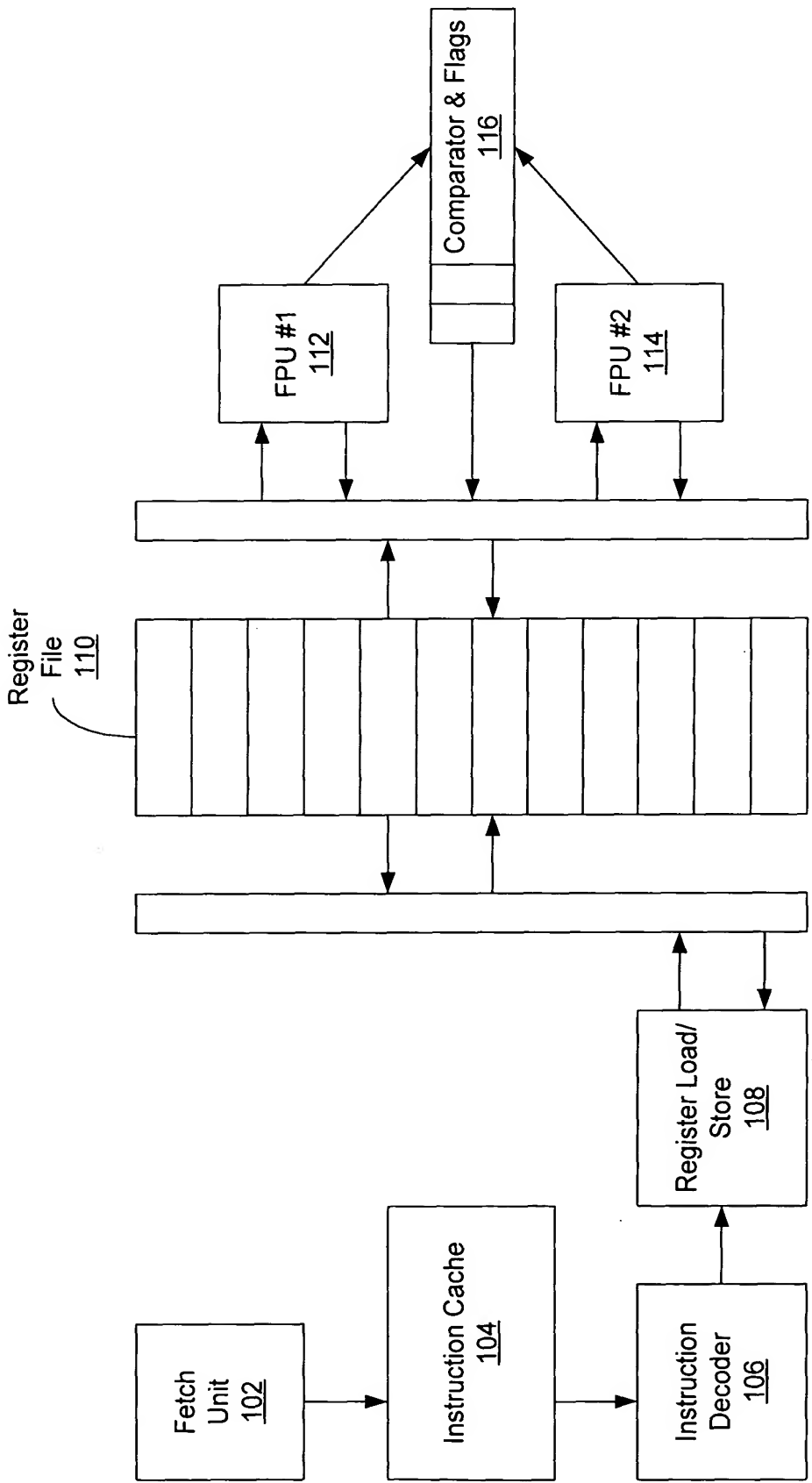Inventor(s): Ken Gary Pomaranski, et al.
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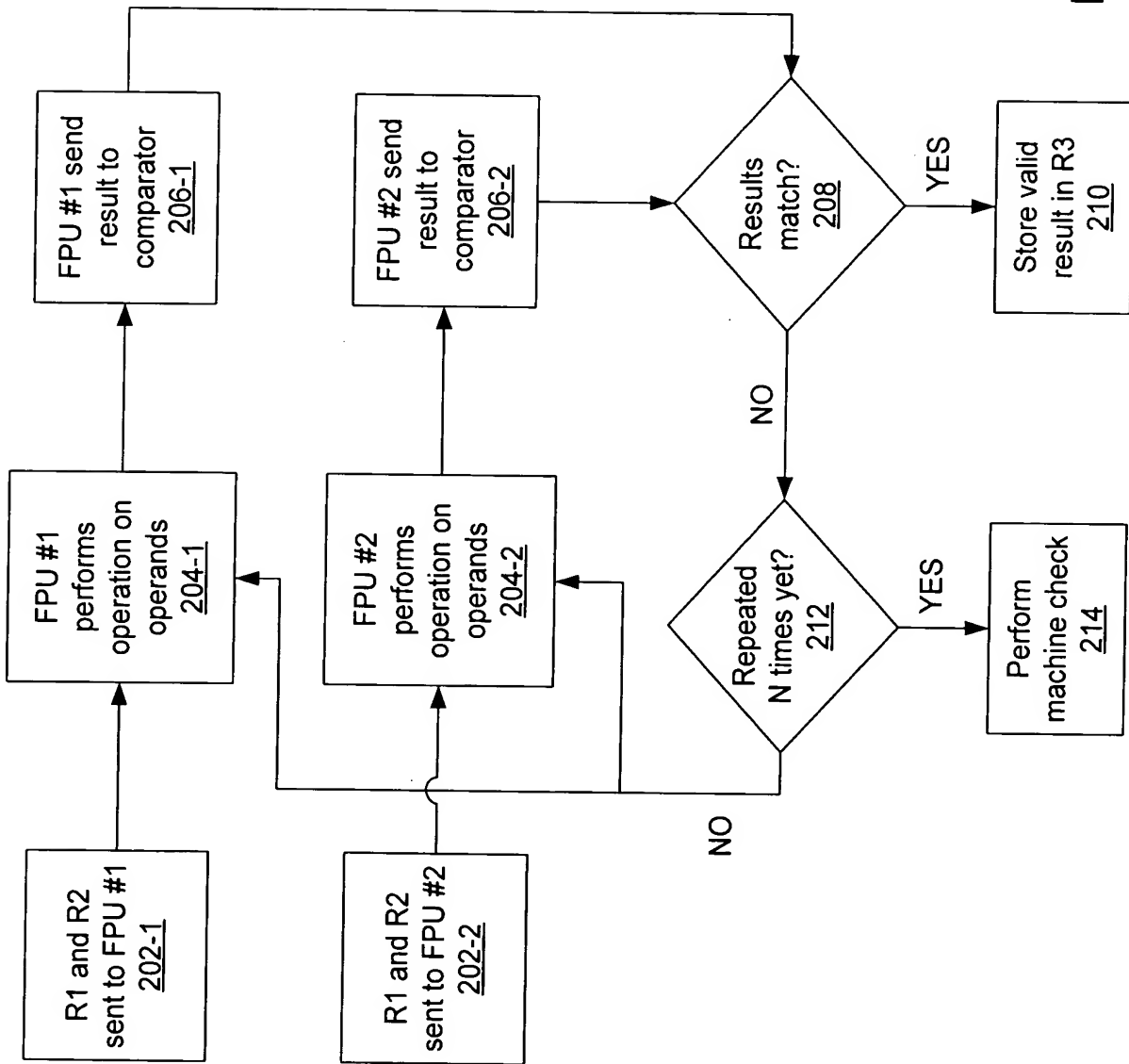Load x -> R1
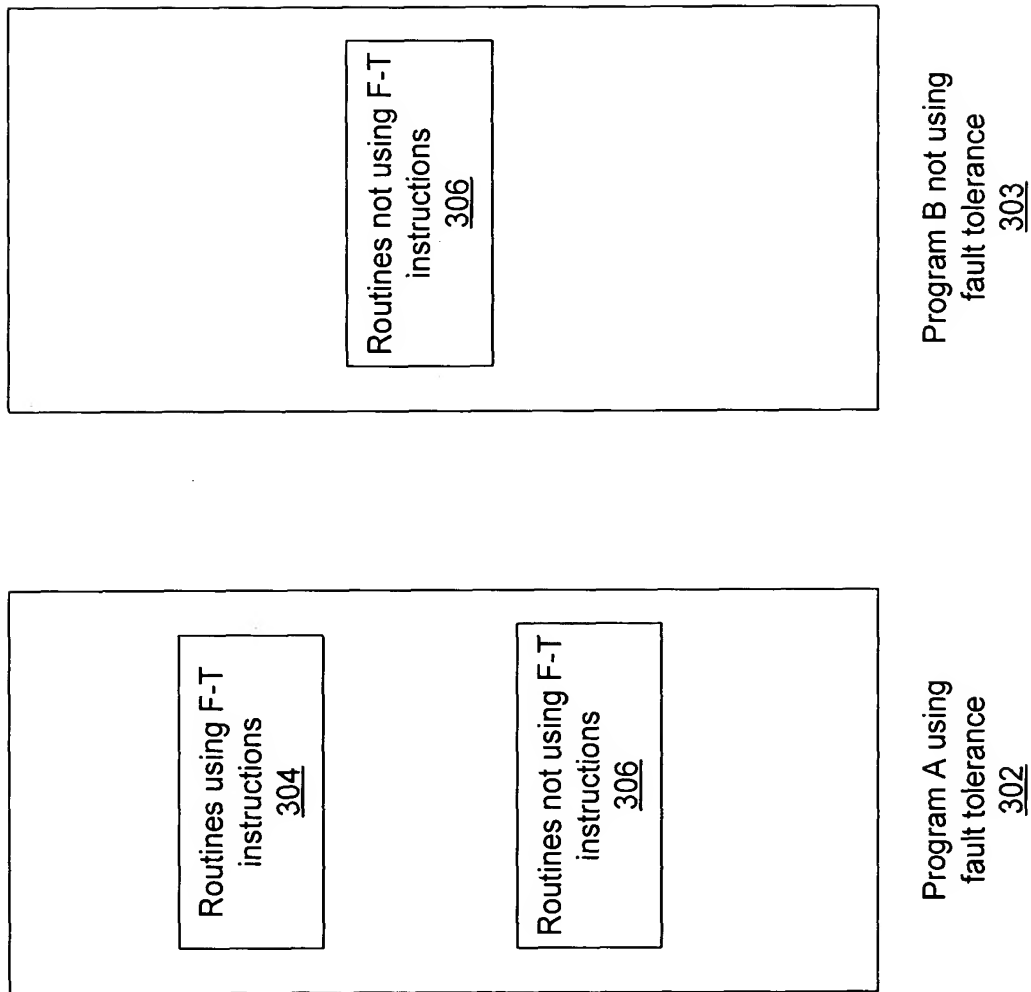Load y -> R2
FT_MULT (R1,R2) -> R3
Store R3

FIG. 2A

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FIG. 2B

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Routines not using F-T instructions
306

Program B not using fault tolerance
303

Routines using F-T instructions
304

Routines not using F-T instructions
306

Program A using fault tolerance
302

FIG. 3